REMARKS

Claims 1-38 are pending in the application.

Claims 33-37 are allowed.

Claims 1-11 and 17-32 are rejected.

Claims 12-16 are objected to.

Claims 3 and 9 have been amended.

Claim 38 has been added.

Objection to the Drawings

FIG. 1B was objected to in the Office Action because all blocks were not labeled with descriptive legends. Submitted with this response is a proposed drawing change, which shows a revised FIG. 1B in which the three previously unlabeled interconnections between nodes have been given reference number 194.

Objections to the Claims

Claim 9 was objected to. This claim has been amended to recite "a clock and data recovery unit". Accordingly, Applicants believe the objection has been overcome.

Rejection of Claims under 35 U.S.C. §103

Claims 1-5, 20-21 and 28-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshifuji, U.S. Patent 5,917,426, in view of Fatehi, et al., U.S. Patent 6,600,581.

With respect to claim 1, the cited art fails to teach or suggest a switching matrix, wherein the switching matrix has a first number of inputs and a second number of outputs; and an error detector, coupled to one of said second number of outputs and configured to generate error information by virtue of being configured to detect errors in an information stream; wherein the switching matrix is configured to receive the information stream at one of the first number of inputs.

As noted in the previous response, Yoshifuji teaches a method involving "connecting a selected one of the input terminals to a selected one of the output terminals through the switch matrix by the use of the connection data signals, monitoring the connection state of the switch matrix, obtaining actual interconnection data signals from the connection state of the switch matrix, and substituting the actual interconnection data signals for the connection data signals when any disorder takes place in connection with the connection data signals." Yoshifuji, col. 1, line 64 – col. 2, line 4. Thus, Yoshifuji teaches substituting the actual interconnection data signals obtained from the connection state for the connection data signals in response to a disorder in the connection data signals, which control the interconnection of input and output terminals. Applicants note that the connection data signals in Yoshifuji are not an information stream received by one of a first number of inputs of a switching matrix. This is recognized by the Examiner on page 4 of the Office Action ("Yoshifuji fails to specially disclose the "*error detector connecting to the outputs and controller to detect error in the information stream*"). Furthermore, there is no suggestion in Yoshifuji to detect errors in an information stream received at an input to the switching matrix, nor would such a suggestion be expected, given Yoshifuji's focus on control signals (the connection data signals and interconnection data signals).

Fatehi teaches a system in which "[v]erification that an optical signal has been properly routed from an input to an output of an optical cross-connect is achieved according to the principles of the invention by tagging an optical signal (e.g., wavelength) with identification information at a cross-connect input, retrieving the identification information from the tagged optical signal at a cross-connect output, and determining from the retrieved identification information whether the optical signal was routed according to a predetermined route." Fatehi, col. 2, lines 47-56. Fatehi tags identification information onto an optical signal at the input to a cross-connect and then removes and verifies this identification information at a cross-connect output. It is noted that unlike the claimed invention, Fatehi's system is dependent on internally-generated error verification information (the "identification information"). Accordingly, the tag read/write elements taught in Fatehi can only verify the internally-generated information, not the information stream that is being tagged with that internally-generated information. Fatehi even teaches away from verifying an information stream, stating that verification can be performed

using the tags while "signal conversions for accessing the payload (e.g., high speed data) are avoided". Fatehi, col. 3, lines 13-14. Thus, Fatehi, both alone and in combination with Yoshifuji, fails to teach or suggest an error detector configured to generate error information by virtue of being configured to detect errors in an information stream. Accordingly, claim 1 is patentable over the cited art for at least this reason. Claims 2-5, 20-21 and 28-30 are patentable over the cited art for similar reasons.

Further with respect to claim 5, the cited art fails to teach or suggest a controller that further configures the switching matrix to couple the one of the first number of inputs to another of the second number of outputs in addition to the one of the second number of outputs to which an error detector is coupled. Both references teach that different connections can be set up between various inputs and outputs of a switching element, and that a given connection can be torn down and a new connection established. However, the references, singly and in combination, fail to teach coupling an input to a particular output in addition to coupling the input to that output to which the error detector is coupled. In other words, neither reference teaches coupling an input to a first output while that input is also coupled to a second output to which an error detector is coupled. Accordingly, claim 5 is further patentable over the cited art for this reason. Claims 21 and 30 are patentable over the cited art for similar reasons.

Claims 6-9, 22 and 31 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshifuji, U.S. Patent 5,917,426, in view of Fatehi, et al., U.S. Patent 6,600,581, and further in view of Al-Salameh, U.S. Patent 6,262,820. These claims are patentable over the cited art for reasons similar to those given above with respect to claim 1.

Further with respect to claim 6, the cited art fails to teach or suggest a system comprising a plurality of receivers, each including a receiver error detector, and a plurality of transmitters, each including a transmitter error detector, wherein an error detector coupled to an output of the switching matrix further localizes a source of errors by virtue of being configured to detect errors occurring after the receiver error detector of each one of the plurality of receivers and before the transmitter error detector of each one of the plurality of transmitters. The Examiner cites the tag read/write elements 211 of Fatehi as teaching both the error detector recited in claim 1 and the

transmitter error detector recited in claim 6 (e.g., see page 7 of the Office Action). However, claim 6 clearly recites that the error detector localizes a source of errors by virtue of being configured to detect errors occurring before the transmitter error detector of each of the plurality of transmitters. Thus, even assuming for the sake of argument that tag read/write elements 211 function in the same way as the claimed error detector and transmitter error detector function individually, tag read/write elements cannot be relied on to teach both of these elements (i.e., a tag read/write element 211 cannot localize errors occurring after a receiver error detector and before a transmitter error detector if the tag read/write element 211 is itself the transmitter error detector). No other portion of the cited art, either alone or in combination with Fatehi, teaches or suggests an error detector that localizes errors by virtue of being configured to detect errors occurring after the receiver error detector of each of the plurality of receivers and before the transmitter error detector of each of the plurality of transmitters. Accordingly, claim 6 is further patentable over the cited art for at least this reason.

With respect to claim 8, the cited art fails to teach or suggest a clock and data recovery unit coupled between said one of said second number of outputs and said error detector. On page 8 of the Office Action, the Examiner cites an internal data memory in Yoshifuji as teaching a clock and data recovery unit. On page 9 of the Office Action, the Examiner cites a counter clock (a millisecond counter clock used to determine if a predetermined threshold time interval has been counted, see Al-Salameh, col. 9, lines 39-42) in Al-Salameh as teaching a clock and data recovery unit. However, the statements that a memory or a counter teach a "clock and data recovery unit" are clearly inconsistent with the meaning one of ordinary skill in the art would give to the phrase "clock and data recovery unit" (e.g., as noted on page 24, lines 21-23 of the specification, a clock and data recovery (CDR) unit can be used as follows: "Switch output 822(17) is fed into a CDR/DEMUX 825, in which the clock is recovered and the input signal demultiplexed from a serial stream into a parallel stream. The CDR is used to re-time the serial data after the data has passed through the crosspoint switch."). A memory and a counter, each considered both alone and in combination with the other portions of the cited art, clearly fail to teach or suggest a clock and data recovery unit. Accordingly, claim 8 is patentable over the cited art.

Claims 10-11, 17-19, 23-27, and 32 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshifuji in view of Fatehi, et al., U.S. Patent 6,600,581, and further in view of Maezawa et al., U.S. Patent 6,145,024. These claims are patentable over the cited art for reasons similar to those given above with respect to claim 1.

Allowable Claims

Claims 12-16 were objected to as being dependent on a rejected base claim and indicated as being allowable if rewritten to include all of the limitations of the base claim and any intervening claims. Claims 12-16 are allowable due to their dependence on an allowable base claim.

Added Claim

Claim 38 has been added. Support for claim 38 can be found on page 24, lines 15-20. Claim 38 is patentable for at least the reasons provided above with respect to claim 5.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is invited to telephone the undersigned at 512-439-5080.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 6, 2004.

Brenna A Brock — 1-6-2004
Attorney for Applicant(s) — Date of Signature

Respectfully submitted,

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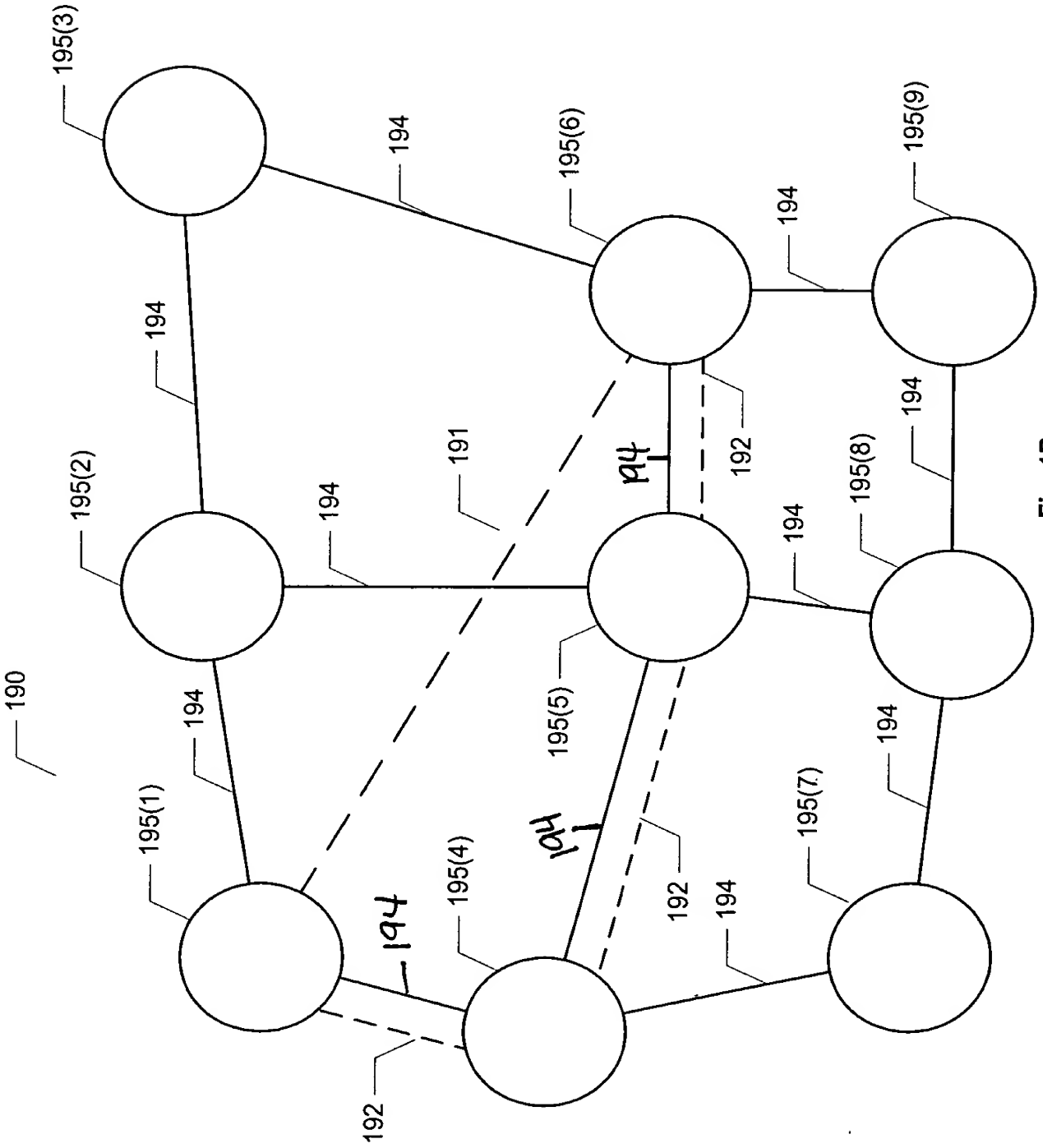

Fig. 1B